



Bardac **drives**

PL / PLX Digital DC Drive
Part 4 Default Block Diagram

Part 1
PL / PLX
Digital DC Drive

Part 2
Application Blocks

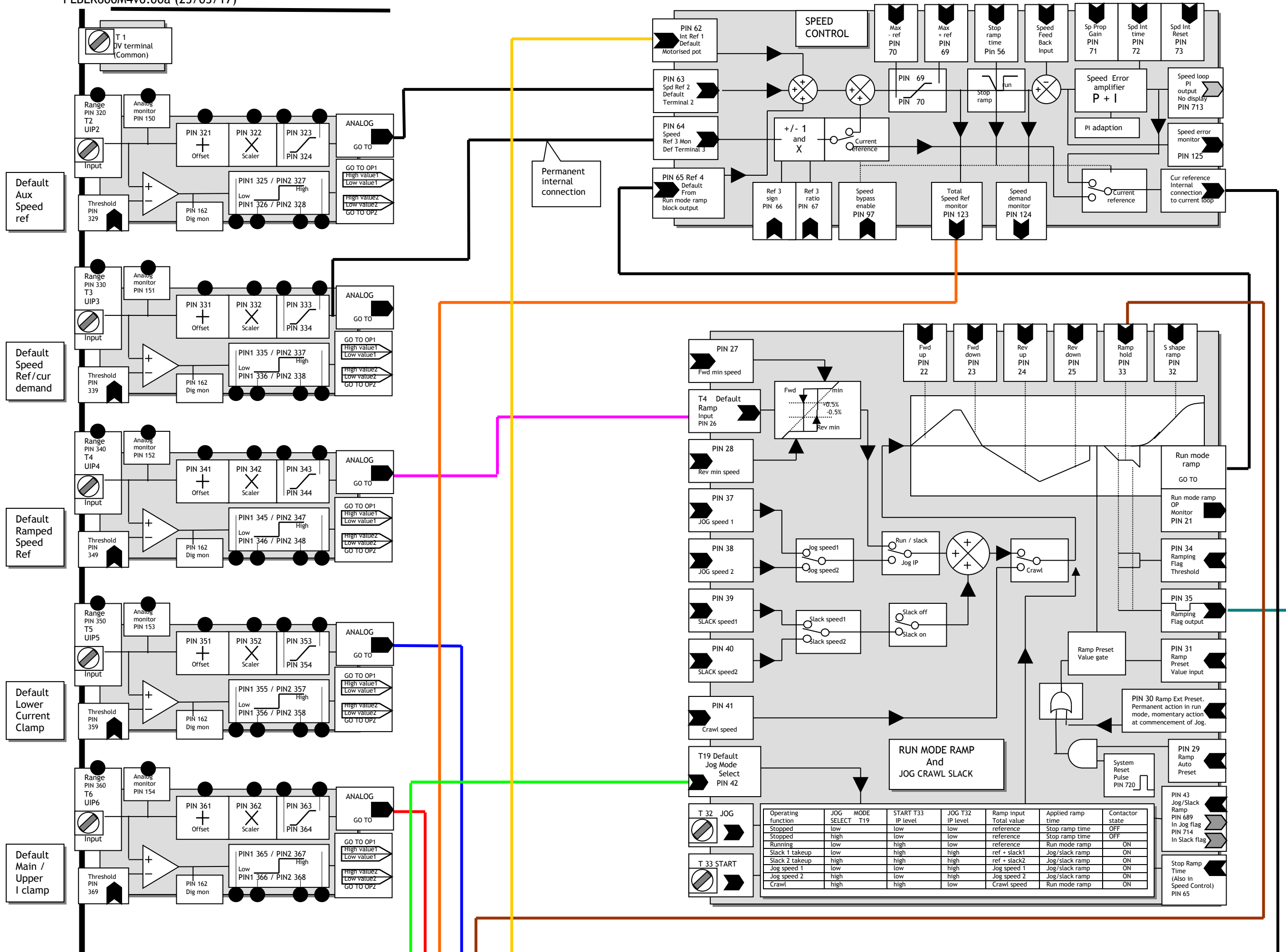
Part 3
High Power Modules
PL / PLX 275 - 980

Part 4
Default Block Diagram



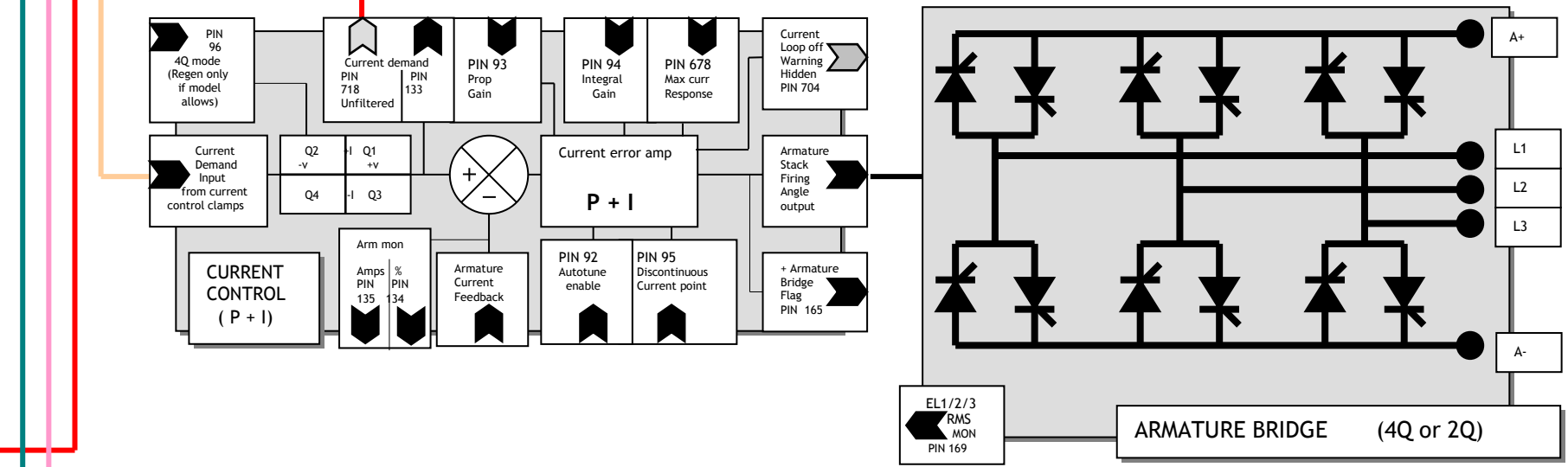
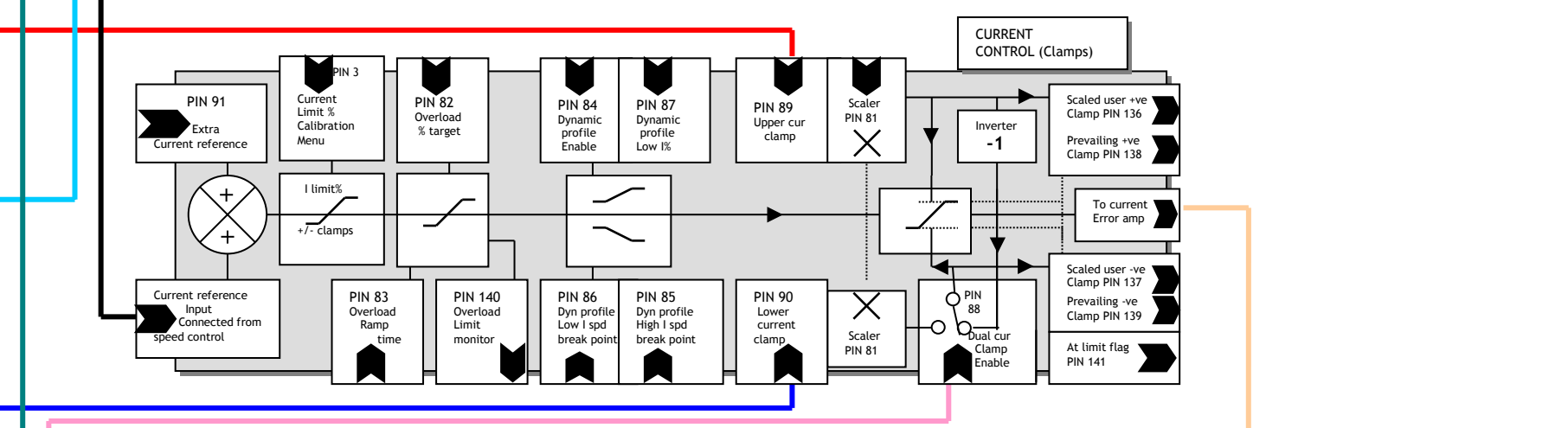
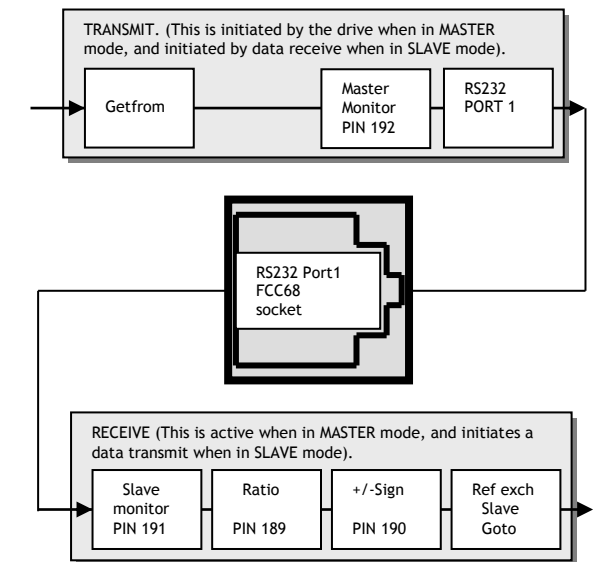
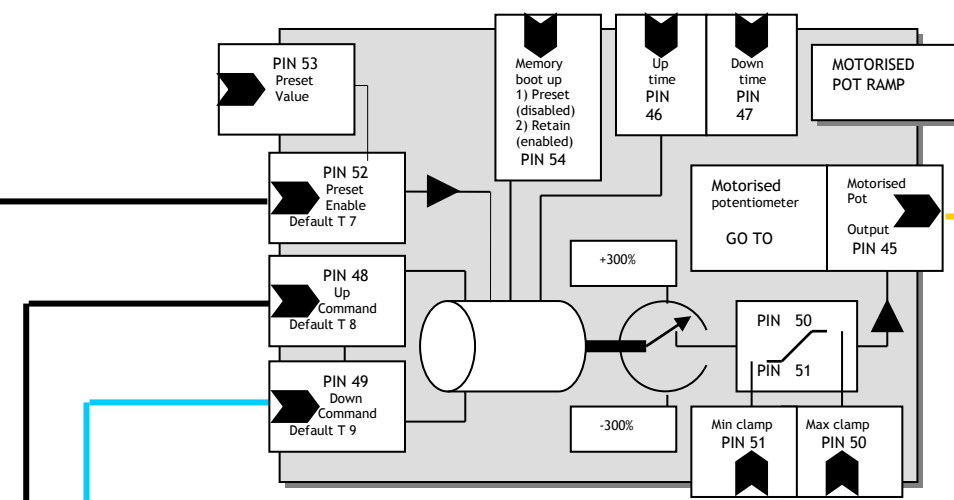
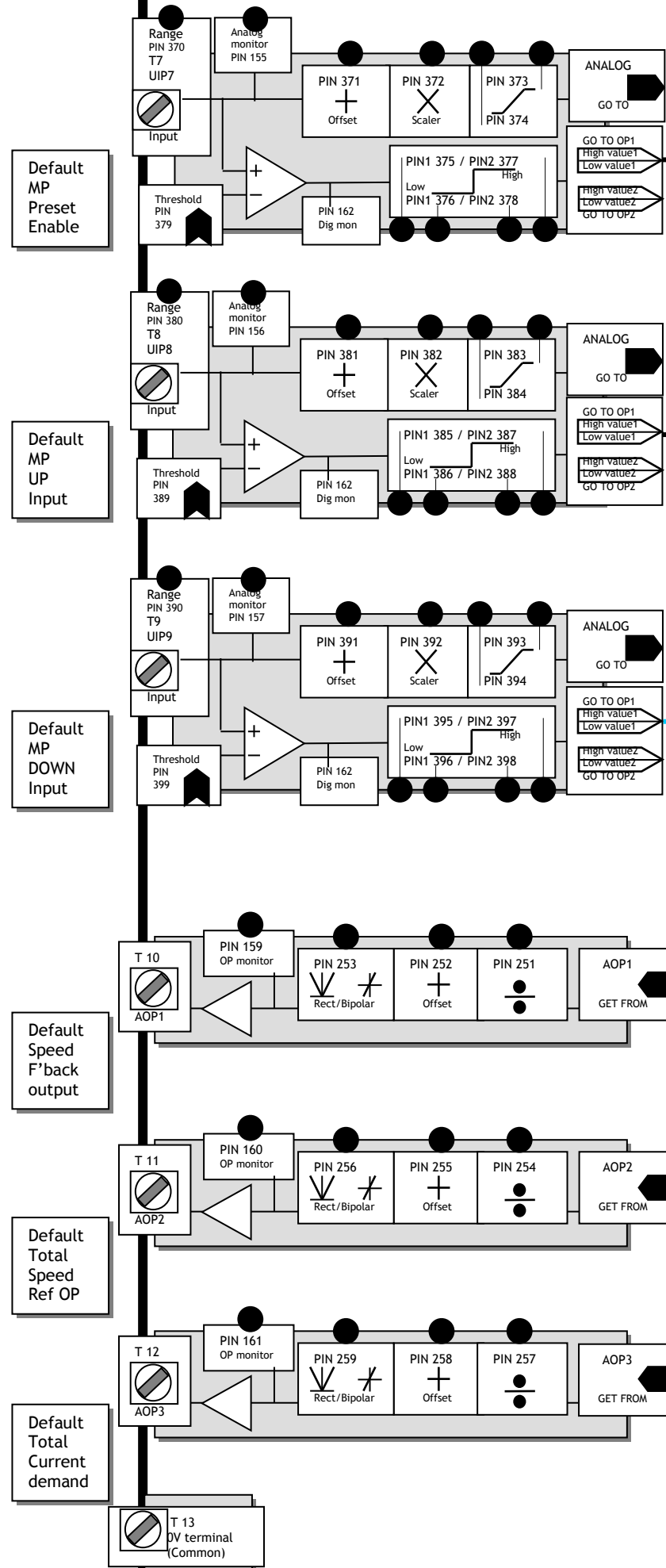
1 Default Block Diagram

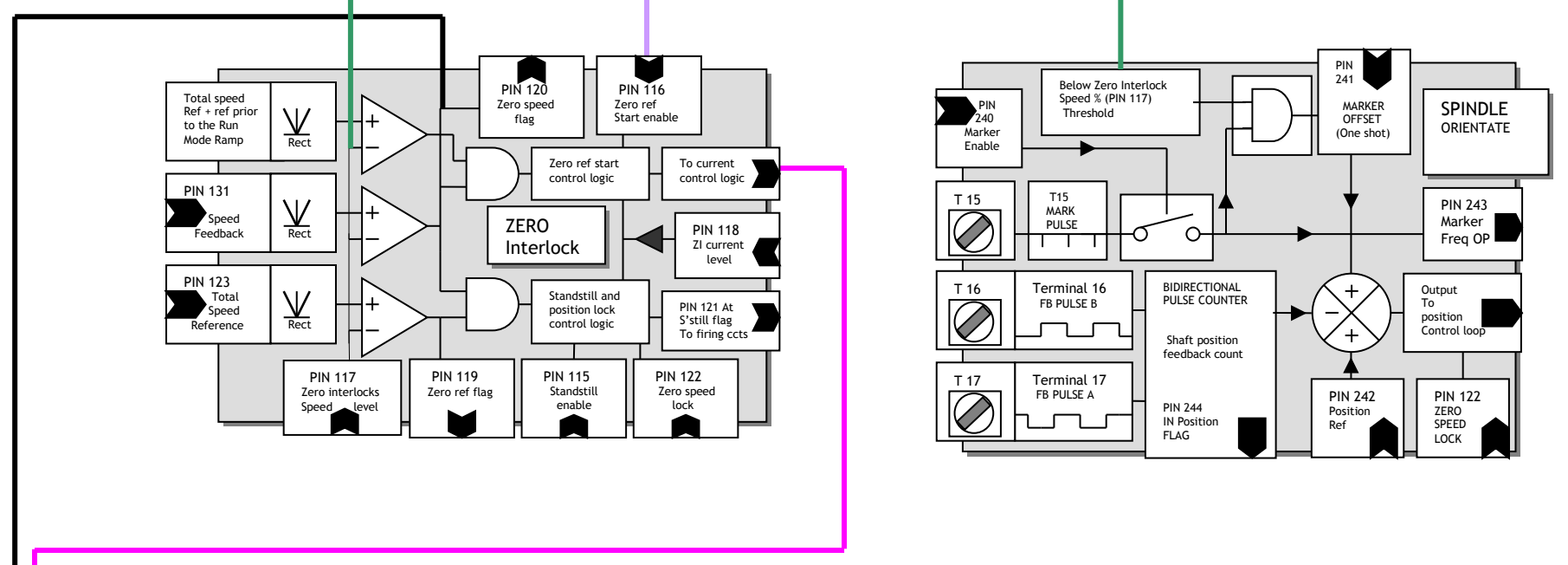
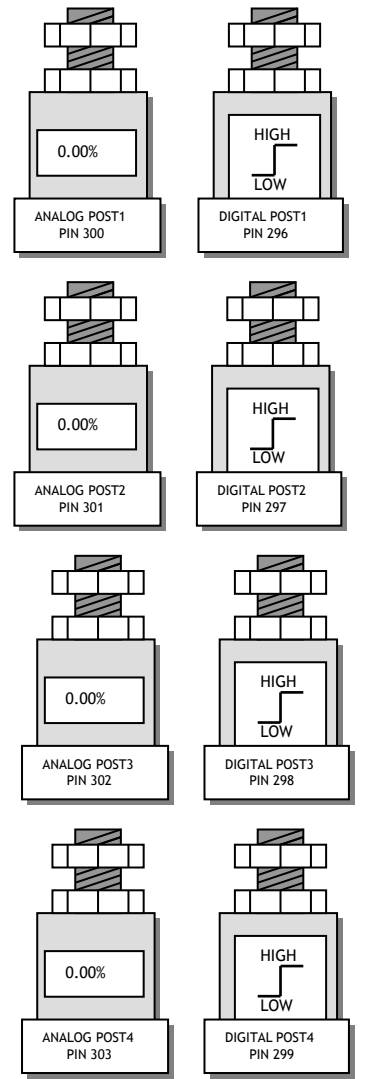
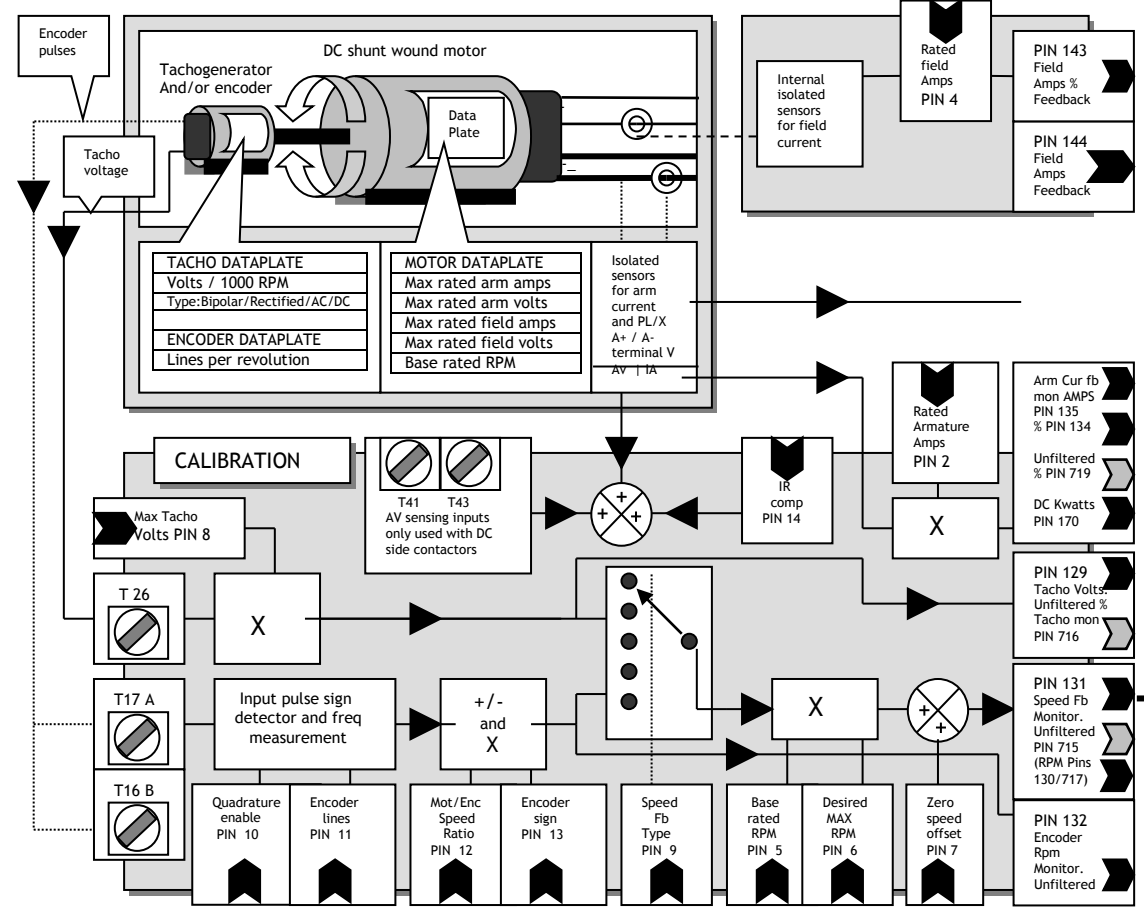
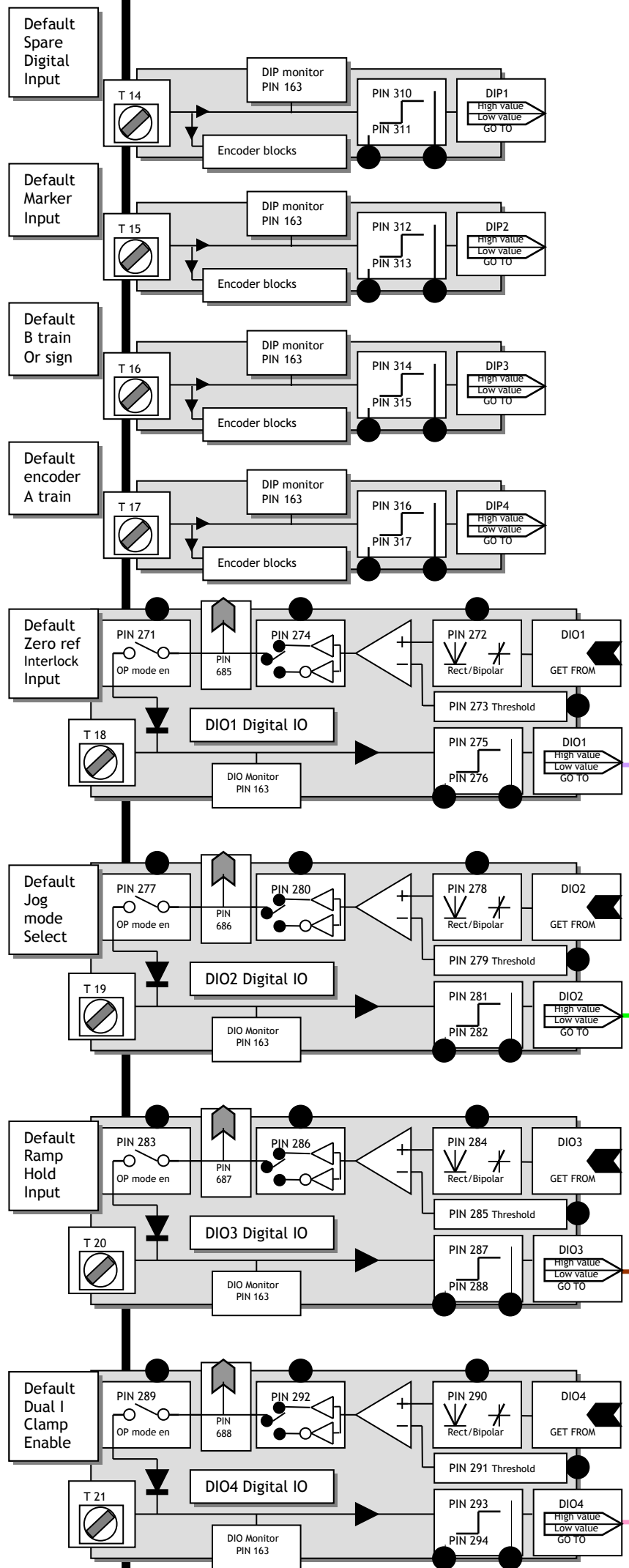
PLBLK600M4v6.00a (23/03/17)

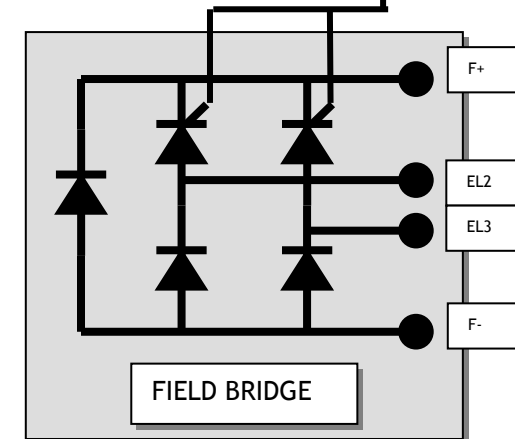
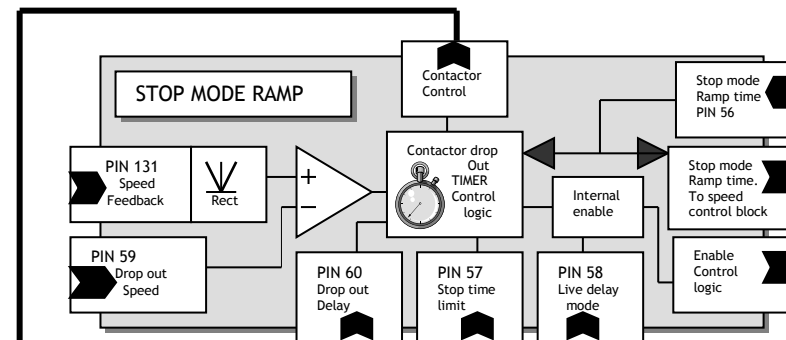
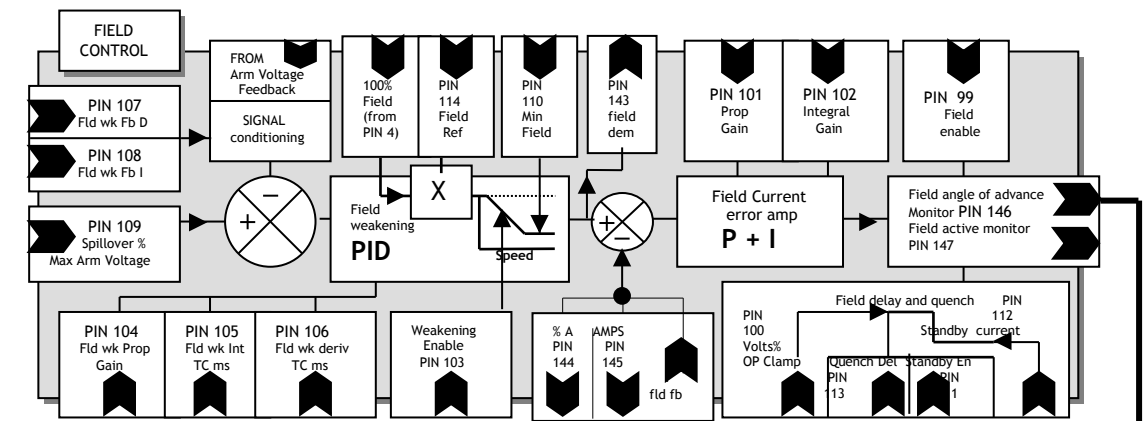
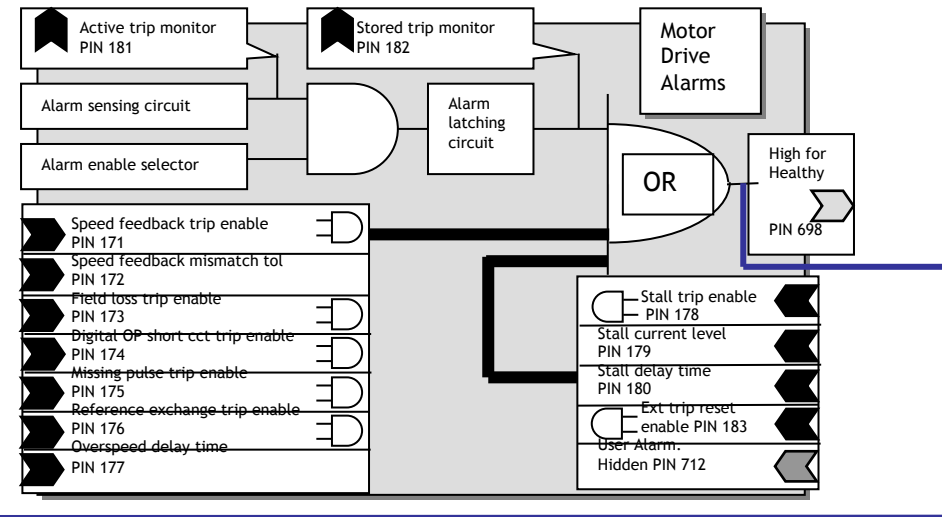
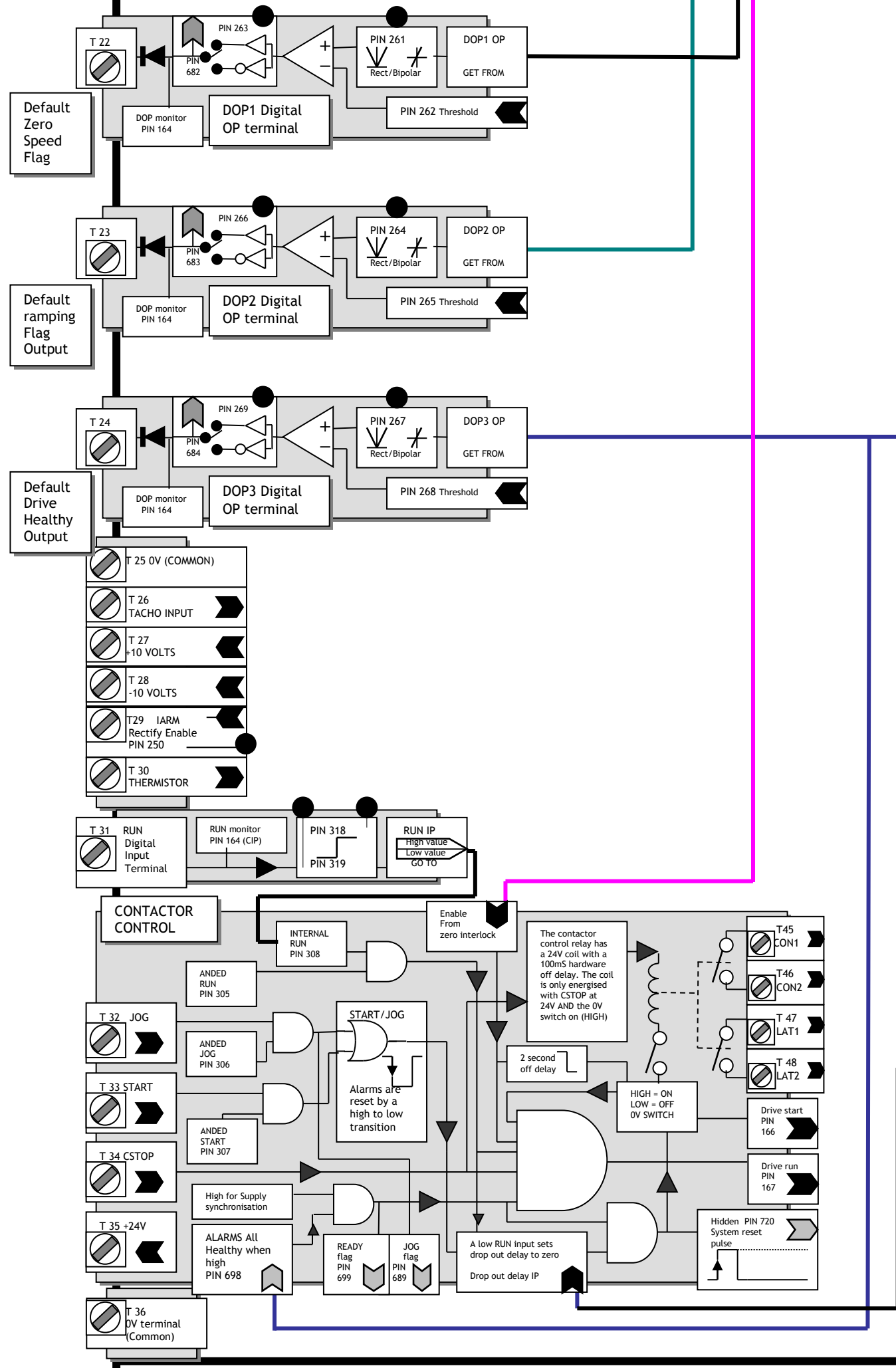


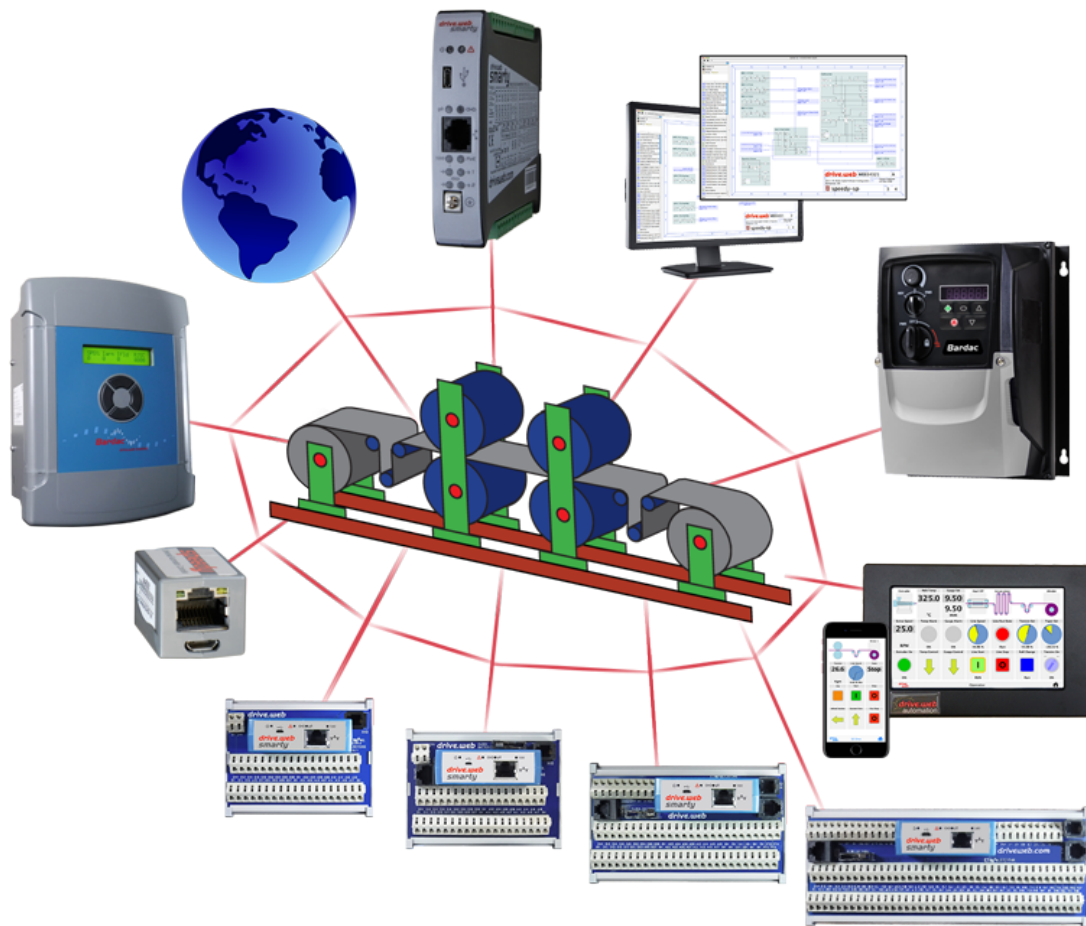
Operating function	JOG MODE SELECT T19	START T33 IP level	JOG T32 IP level	Ramp input Total value	Applied ramp time	Contactors state
Stopped	low	low	low	reference	Stop ramp time	OFF
Stopped	high	low	low	reference	Stop ramp time	OFF
Running	low	high	low	reference	Run mode ramp	ON
Slack 1 takeover	low	high	high	ref + slack1	Jog/slack ramp	ON
Slack 2 takeover	high	high	high	ref + slack2	Jog/slack ramp	ON
Jog speed 1	low	low	high	Jog speed 1	Jog/slack ramp	ON
Jog speed 2	high	low	high	Jog speed 2	Jog/slack ramp	ON
Crawl	high	high	low	Crawl speed	Run mode ramp	ON

Default block diagram 2









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